Claims

Having thus described our invention, what we claim as new and desire to secure by Letters Patents is.

1. A method of processing instructions in a computer system, said method comprising:

determining if the number of outstanding write instructions issued from said processor and targeted to a designated region of memory is above a threshold; and

issuing a fence instruction designating said region of memory, where no further instructions are issued from said processor until said number of outstanding writes targeted to said designated region is below said threshold.

2 . A apparatus for processing instructions in a computer system, said method comprising:

an issue unit for determining if the number of outstanding write instructions issued from said processor is above a threshold, and for issuing a fence instruction designating a region of memory, where no further instructions are issued from the processor until said number of writes to said designated region is below said threshold.

3. An apparatus as recited in claim 2, wherein said device is a counter.

4. A system for processing instructions, said system comprising:

a memory for storing data;

an issue unit for, in response to each of a number of instructions, retrieving operand data from said memory, and for forwarding, without storing in said memory or in said issue unit, an op code of said each instruction and a target location of said each instruction; and

an execution unit for executing each of said number of instructions by operating on said data in accordance with said op code and for storing results of said operation on said data at a location in said memory specified by said target location, wherein said target location, said op code and said operand data are received by said execution unit.

5. A method of processing instructions in a computer system, said method comprising:

in response to each of a number of said instructions:

retrieving operand data from a memory, and forwarding said operand data, an op code, and a target location to an execution unit associated with said system; and

executing each instruction by operating on said operand data in accordance with said op code and storing results of said operation on said operand data at a location in said memory specified by said target location.

6. A method of processing memory instructions in a computer system, said method comprising:

in response to each of an number of memory instructions:

retrieving operand data from a memory, and forwarding said operand data, an op code, and a target location to an execution unit associated with said system, and executing each instruction by operating on said operand data in accordance with said op code and storing results of said operation on said operand data at a location in said memory specified by said target location; and

issuing fence instructions designating a region of memory, where no further instructions are issued from the processor until a number of writes to said designated region is below said threshold.

7. A system for processing instructions, said system comprising:

a memory for storing data;

an issue unit, in response to each of a number of memory instructions, for retrieving operand data

from said memory, an op code of said each memory instruction and a target location of said each memory instruction;

an execution unit for executing each of said number of memory instructions by operating on said data in accordance with said op code and for storing results of said operation on said data at a

location in said memory specified by said target location, wherein said target location, said op code and said operand data are received by said execution unit from said issue unit through said memory; and

said issue unit also issuing fence instructions for designating regions of memory, wherein for each of said designated regions, no further memory instructions are issued until a number of outstanding writes to said each region is below a corresponding threshold.

8. A method of processing instructions in a computer system, said method comprising:

when a memory instruction is issued from a processor of said system, incrementing a counter associated with a memory region that contains a memory location specified by a target address of said issued instruction, each memory instruction for reading data from and writing data into a memory;

when a memory instruction is executed by a processor of said system, decrementing a counter associated with a memory region that contains a memory location specified by a target address of said executed instruction; and

issuing a fence instruction designating a region of memory, where no further instructions are issued until said counter associated with said designated region is below a threshold.

9. A apparatus for processing instructions in a computer system, said apparatus comprising:

when a memory instruction is issued from a processor of said system, incrementing a counter associated with a memory region that contains a memory location specified by a target address of said issued memory instruction, each memory instruction for reading data from and writing data into a memory;

when a memory instruction is executed by a processor of said system, decrementing a counter associated with a memory region that contains a memory location specified by a target address of said executed instruction; and

issuing a fence instruction, where no further instructions are issued until said counter associated with said designated region is below a threshold.

10. A method of processing instructions in a computer system, said method comprising:

when an instruction is issued from a processor of said system, incrementing a counter associated with a memory region that contains a memory location specified by a target address of said issued instruction, each instruction for reading data from and writing data into a memory;

when a memory instruction is executed by a processor of said system, decrementing a counter associated with a memory region that contains a memory location specified by a target address of said executed instruction, wherein each issued instruction includes data retrieved from said memory, an op code and target location; and

issuing a fence instruction designating a region of memory, where no further instructions are issued until said counter associated with said designated region is below a threshold.

11. A apparatus for processing instructions in a computer system, said apparatus comprising:

when an instruction is issued from a processor of said system, incrementing a counter associated with a memory region that contains a memory location specified by a target address of said issued instruction, each instruction for reading data from and writing data into a memory;

when an instruction is executed by a processor of said system, decrementing a counter associated

with a memory region that contains a memory location specified by a target address of said executed instruction, wherein each issued instruction includes data retrieved from said memory, an op code and target location, so that each issued instruction can be executed independently of any information not included in each issued instruction; and

issuing a fence instruction designating a region of memory, where no further instructions are issued until said counter associated with said designated region is below a threshold

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